Customer No.: 26021

Amendments to the Specification:

Please replace the title with the following rewritten title:

DATA PROCESSING DEVICE AND ELETRONIC EQUIPMENT <u>USING</u> PIPELINE CONTROL

Please replace the abstract with the following rewritten abstract:

A data processing device using pipeline architecture which enables to reduces a time loss due to a branch without causing an increase in circuit scale. The data processing device uses pipeline control. The data processing device includes an instruction queue in which a plurality of instruction codes can be fetched, a fetch address operation circuit which calculates a fetch address, a fetch circuit which fetches an instruction code based on the fetch address, and a branch information setting circuit which decodes a branch setting instruction, stores a branch address in a branch address storage register, and stores a branch target address in a branch target address storage register. The fetch address operation circuit compares either a previous fetch address or an expected next fetch address with a value stored in the branch address storage register, and determines a next fetch address to be output, based on the comparison result.

Please replace the paragraph beginning at page 12, line 10 with the following rewritten paragraph:

The CPU 10 includes a fetch circuit 20, a fetch address operation circuit 40, a decoder circuit 60, an execution circuit 70, a register file 80 (general-purpose register 82 and special register 84), an instruction address generator 90, and the like.

Attorney Docket No. 81751.0061 Customer No.: 26021

Please replace the paragraph beginning at page 13, line 5 with the following rewritten paragraph:

The fetch address operation circuit 40 may output the value stored in the branch target address storage register 42 44 as the next fetch address based on the comparison results until the number of branches to the branch target address reaches a loop count.

Please delete the paragraph beginning at page 14, line 8-11.